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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 10/079,651
Filing Date: February 20, 2002
Appellant(s): CAMPISANO ET AL.

Marshall Curtis
Reg. No. 33,138
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 10/1/07 appealing from the Office action mailed 11/15/06.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 7,006,588 | Simmons et al | 2-2006 |
| 5,668,599 | Cheney et al | 9-1997 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons et al. (7006588), (hereinafter referred to as "Simmons").

Regarding claim 1, Simmons discloses an apparatus that relates to synchronization detection (Simmons: column 1, lines 17-19). This apparatus comprises "determining a frame switch point in accordance with a signal corresponding to the completion of decoding of a previous frame" (Simmons: column 5, lines 21-24, column 5, lines 46-50, wherein the frame switch point is the FS pattern) and "synchronizing the video decoder for decoding image data in accordance with the frame switch point" (Simmons: column 5, lines 46-50, wherein the decoder decodes one frame of image data upon the detection of the FS pattern). Although Simmons fails to use the term "frame switch point", Simmons does disclose a FS pattern which is shown in figures 4-5 to indicate the switch between frames. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the FS pattern in order to obtain an apparatus that correctly identifies the transition between images or frames.

2. Claims 2-5, 7-12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simmons et al. (7006588), (hereinafter referred to as "Simmons") in view of Cheney et al. (5668599), (hereinafter referred to as "Cheney").

Regarding claims 2 and 9, note the examiners rejection for claim 1, and in addition, claims 2 and 9 differ from claim 1 in that claims 2 and 9 further require a spill buffer and controlling decoder latency according to the spill buffer. Cheney teaches that a spill buffer is needed to minimize memory requirements when decoding B frames (Cheney: column 14, lines 16-27). Cheney further discloses "altering decoder latency in response to the spill buffer" (Cheney: column 14, lines 36-44, wherein altering the latency is the process of holding back the decoding). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to take the apparatus disclosed by Simmons and add the spill buffer taught by Cheney in order to obtain a more cost efficient apparatus by minimizing memory requirements.

Regarding claims 3 and 10, Cheney discloses "reconfiguring a frame buffer to accommodate an increased latency of motion video data scaled in the decoding path" (Cheney: column 14, lines 25-44, wherein reconfiguring the frame buffer is the process of detecting the frame buffer size and switching between the frame and spill buffers as needed).

Regarding claims 4-5 and 11-12, Cheney discloses "continuously scaling video from the motion video data by interpolation" (Cheney: figure 5, column 9, lines 66-67 – column 10, lines 1-5, wherein the interpolation is performed by the motion compensation unit).

Regarding claims 7-8 and 14-15, Cheney discloses "the spill buffer has a capacity equal to or less than one field" Cheney: figure 15, column 15, lines 1-31).

**(10) Response to Argument**

i. On pages 18-22, appellant argues that Simmons fails to disclose determining a frame switch point and synchronizing a decoder in accordance with one of display of a bottom border of a scaled image and the frame switch point.

The examiner notes that synchronizing a decoder in accordance with one of a display of a bottom border of a scaled image and a frame switch point indicates a claim in the alternative form. Accordingly, the examiner has interpreted the claim to read synchronizing a decoder in accordance with the frame switch point. Simmons discloses in column 5, lines 14-25, the use of frame synchronization (FS) pattern. Upon detection of the FS pattern Simmons discloses in column 5, lines 45-50, entering a decode state and completely decoding a frame of data. When the decoding is finished, the receiver reverts back to the FS search state. Since a full frame is decoded based upon the detection of the FS pattern, the FS pattern indicates a point where different frames occur (where the frames are switched). Hence, Simmons discloses determining a frame switch point and synchronizing a decoder in accordance with one of display of a bottom border of a scaled image and the frame switch point.

ii. On pages 22-23, appellant argues that Cheney fails to disclose testing spill buffer capacity responsive to a test result and controlling scaling in a decoding path and altering decoder latency in response to the result.

Cheney discloses in column 14, lines 30-44, the use of a spill buffer. The hardware automatically detects whether a buffer's logical address exceeds the buffer size and steers the address to point to the spill buffer. Hence, the hardware would have to perform a test to determine if the buffer size has been exceeded. Cheney further discloses holding back the decoding until the display process is beyond the point of conflict. Since the decoding is held back, Cheney is altering the decoder latency. Hence, Cheney discloses disclose testing spill buffer capacity responsive to a test result and controlling scaling in a decoding path and altering decoder latency in response to the result.

iii. On page 24, appellant argues that Cheney fails to disclose reconfiguring the frame buffer for accommodating an increased latency.

Cheney discloses in column 14, lines 30-35, wrapping the logical address from the spill buffer into the frame buffer. By wrapping the logical address, Cheney is reconfiguring, or changing, the frame buffer to accept data at various points. Cheney further discloses in column 14, lines 54-67, varying an index position to adjust the storage locations of the buffer, thereby reconfiguring or changing the buffer. Hence, Cheney discloses reconfiguring the frame buffer for accommodating an increased latency.

iv. On pages 24-25, appellant argues that Cheney fails to disclose continuous scaling from motion video data.

Cheney illustrates in figure 5 and discloses in column 3, lines 7-16, reducing spatial redundancy by using scalar quantization. By using scalar quantization, Cheney is continuously scaling the video data. Further the examiner notes that scaling video data is well known within the MPEG environment and helps reduce the amount of video data the needs to be processed by a system and transmitted over a network. Hence, Cheney discloses continuous scaling from motion video data.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

**(12) Evidence Appendix**

No evidence has been submitted by appellant.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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